REMARKS

In the Office Action, the Examiner indicated that claims 1 through 34 are pending in the application, that claims 1-7 and 9-34 are rejected, and that claim 8 is objected to.

Allowable Subject Matter

On page 16 of the Office Action, the Examiner indicated that claim 8 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicant thanks the Examiner for this indication of allowable subject matter.

Claim Rejections, 35 U.S.C. §§102 and 103

On page 2 of the Office Action, the Examiner again rejected claims 1-5, 9-11, 23, 25-27, 30-32, and 34 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 4,847,755 to Morrison.

On page 8 of the Office Action, the Examiner has again rejected claims 6-7, 24, 28-29, and 33 under 35 U.S.C. §103(a) as being unpatentable over Morrison. On page 12 of the Office Action, the Examiner has rejected claims 12-18 under 35 U.S.C. §103(a) as being unpatentable over Morrison in view of U.S. Patent No. 6,289,442 to Asato. On page 14 of the Office Action, the Examiner has rejected claims 19-21 under 35 U.S.C. §103(a) as being unpatentable over Morrison in view of U.S. Patent No. 7,055,021 to Kadambi. Finally, on page 15 of the Office

Action, the Examiner has rejected claim 22 under 35 U.S.C. § 103(a) as being unpatentable over Morrison in view of Kadambi and further in view of U.S. Patent No. 5,193,180 to Hastings.

Applicant's Response to Examiner's "Response to Arguments"

On pages 16 -18 of the Office Action, under the heading "Response to Arguments", the Examiner lists three bases for maintaining the rejection of the claims. Applicant first addresses the second and third bases, set forth in paragraphs 48 - 51 on pages 17 and 18.

In paragraphs 48 and 49, the Examiner asserts that claim language supporting Applicant's argument, that out-of-order execution of instructions across basic blocks is not taught or suggested by prior art, is not in the claims. In paragraphs 50 and 51, the Examiner asserts that the claim language supporting Applicant's argument, that instructions from different strands can be mixed freely in the instruction schedule, is not claimed. In response, Applicant has amended claim 1 so that it now explicitly states that there are a sequence of operations from a single execution thread *and across multiple basic blocks* and that they are divided into individual strands, and that *instructions from different basic blocks are assigned to different strands*. This provides support in the claims for the arguments noted by the Examiner, and it is thus believed that the claims, as amended, patentably define over the prior art.

Turning to the first basis for maintaining the rejection of the claims, Applicant believes that the above-mentioned claim amendments renders this basis moot. However, Applicant notes that the term "strand numbering" is clearly defined in the application as filed; see the second paragraph on page 3 of the application as filed. When reference is made to the specification to

determine the meaning of claim language, as is required, it is a simple matter to compare the term "strand numbering" as claimed to the "instruction numbering" in Table 5 of Morrison, and determine that the two numbering schemes are non-analogous.

For the Examiner's convenience, Applicant sets forth again, below, the arguments presented in the previous response. In view of the claim amendments presented herein, Applicant believes the claims are in allowable condition.

Restatement of Previous Arguments (Resubmitted for Examiner's Convenience)

The Examiner's reliance on Morrison to reject the claims is based on the incorrect analogizing of the claimed "strand numbering" to the "instruction numbering" of Morrison. For instance, the examiner draws an equivalence between the claimed strand numbering and the instruction numbering of Table 5 in column 12 of Morrison. However, they are not the same; Morrison's numbering is of individual instructions *within* each basic block whereas the strand number is a number of multiple instructions *across* basic blocks. Thus, with the present claimed invention multiple instructions (typically within the same basic block) can be given the same strand number, whereas in Morrison's approach each individual instruction is given a different number. This is a key difference as the claimed strand approach provides a mechanism to label multiple instructions with a common conditionality or predicate status. This is neither taught nor suggested by Morrison.

The Examiner also states that operations in Morrison may be performed out of order with respect to their numbering. This is indeed the case, but in Morrison this corresponds to out of

order instruction execution *within* a basic block. In the present claimed invention (since strand numbers are typically associated with different basic blocks) this corresponds to out of order issue both within *and across* basic blocks. In particular, Morrison, column 20, lines 15-25, describes how instructions in different basic blocks are specifically labeled with disjoint numbers so that there is no mixing of instructions across the basic blocks. The strand numbering of the present claimed invention specifically, and advantageously, allows mixing of instructions across basic blocks, as it enables parallelism to be exploited over a wider program scope.

The Examiner also states that instruction I5 from column 8, Table 1 is a branch that is used to determine the completion status for subsequent instructions. However this is not due to a predication state associated with the strand number (as claimed in the present invention) but because the subsequent instructions from the repeated basic block are not fetched if the branch is not taken. In other words, this approach of Morrison is a well known prior art control-based mechanism. The strand mechanism of the claimed invention is a data flow predication mechanism that associates a single predicate status with a previously labeled set of instructions sharing the same strand number. This is advantageous as it allows instructions from different strands (and thus basic blocks) to be mixed freely in the instruction schedule. For instance, if the loop of the Morrison example contained a conditionally executed instruction, then this would break the loop into multiple basic blocks. Instructions from the next basic block cannot be executed until the branch is resolved and all instructions from the previous basic block are completed (as discussed in the BEU delay mechanism of Column 13, lines 7 - 42). No parallelism exists between the basic blocks.

In the approach of the present invention, by way of contrast, instructions with a strand number for the conditional basic block can be freely scheduled in time as long as the final predicate status for the strand is calculated prior to the execution of any instruction from the conditional strand that affects the final machine state. This capability greatly increases the scope for parallel instruction execution, and cannot be achieved by Morrison.

Independent claim 1 includes specific recitation of the strand numbering and other elements stated above that are not taught or suggested by Morrison. Thus, each of the dependent claims are patentable over Morrison for the same reasons as set forth above with respect to claim 1. Further, the remaining references cited by the examiner also fail to teach or suggests the limitations missing from Morrison. As such, the claims patentably define over all of the cited references, taken alone or in combination. Accordingly, the Examiner is respectfully requested to reconsider and withdraw the rejection of the claims under 35 U.S.C. §§102 and 103.

Conclusion

In view of the foregoing amendments and remarks, applicant respectfully requests entry of the amendments, favorable reconsideration of the application, withdrawal of all rejections and objections and that claims 1 - 34 be allowed at an early date and the patent allowed to issue.

The Commissioner is hereby authorized to charge any fees associated with this communication to Deposit Account No. 50-4364.

Respectfully submitted

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